IN THE CLAIMS

For the convenience of the Examiner, all pending claims of the present Application are shown below whether or not an amendment has been made.

Please amend the claims as follows.

1. **(Currently amended)** A time slot interchanger (TSI) for a telecommunications node, comprising:

an exchange memory **comprising** ~~**including**~~ a plurality of exchange memory slots, each exchange memory slot sized to store a traffic channel and **comprising** ~~**including**~~ a plurality of discretely addressable fields sized to store a sub-channel; and

a controller operable in response to predefined switching instructions to write a sub-channel received in a first **channel** ~~**time slot**~~ to a first field in a memory slot and to write a sub-channel received in a second **channel** ~~**time slot**~~ to a second field in the memory slot**, so that the sub-channel written to the first field and the sub-channel written to the second field may be read from the memory slot as a single traffic channel**.

2. **(Original)** The TSI of Claim 1, the controller further operable to read a first sub-channel from a memory slot to an egress time slot and a second sub-channel in the memory slot to a disparate egress time slot.

3. **(Currently amended)** The TSI of Claim 1, the controller further operable to write a first sub-channel **of a first channel stored** in a memory slot to a ~~**first**~~ disparate memory slot **associated with a second channel** and to write a second sub-channel **of the first channel** ~~**in the memory slot**~~ to a ~~**second**~~ disparate memory slot **associated with a third channel**.

4. **(Original)** The TSI of Claim 1, the controller further operable to write a sub-channel in a field of a memory slot to a disparate field in a memory slot.

5. **(Original)** The TSI of Claim 1, the controller further operable to write a sub-channel in a field of a memory slot to a disparate field in an egress time slot.

6. **(Original)** The TSI of Claim 1, wherein the traffic channel is a DS-0 and the sub-channel is a ¼ DS-0.

7. **(Currently amended)** The TSI of Claim 1, further comprising:

the exchange memory comprising an exchange random access memory (RAM) and an exchange register bank;

the exchange RAM **comprising** ~~**including**~~ a plurality of exchange RAM slots each sized to store the traffic channel and **comprising** ~~**including**~~ a plurality of discretely addressable fields sized to store a sub-channel; and

the exchange register bank **comprising** ~~**including**~~ a plurality of exchange registers each sized to store the traffic channel and **comprising** ~~**including**~~ a plurality of discretely addressable fields sized to store a sub-channel.

8. **(Original)** The TSI of Claim 7, the controller operable to write a sub-channel in an exchange RAM slot to a first field in an exchange register and to write a sub-channel in a disparate exchange RAM slot to a second field in the exchange register.

9. **(Original)** The TSI of Claim 7, the controller further operable to write a first sub-channel in an exchange RAM slot to a first exchange register and to write a second sub-channel in the exchange RAM slot to a second exchange register.

10. **(Original)** The TSI of Claim 7, the controller further operable to write a sub-channel in a field of an exchange RAM slot to a disparate field in an exchange register.

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11. **(Original)** The TSI of Claim 7, wherein the exchange register is internal to the controller.

12. **(Currently amended)** A method for time division multiplex (TDM) switching of traffic in a telecommunications node, comprising:

receiving a traffic stream **comprising** ~~**including**~~ a plurality of traffic channels having discrete sub-channels;

writing a first traffic channel that includes a first sub-channel to a first memory slot in an exchange memory;

writing a second traffic channel that includes a second sub-channel to a second memory slot in an exchange memory;

~~**writing each traffic channel to a separate memory slot in an exchange memory**~~;

writing **the first sub-channel** ~~**a sub-channel in a first memory slot**~~ to a first field in a **third** ~~**second**~~ memory slot;

writing **the second sub-channel** ~~**a sub-channel in a third memory slot**~~ to a second field in the **third** ~~**second**~~ memory slot; and

reading ~~**a combined traffic channel including**~~ the sub-channels from the **third** ~~**second**~~ memory slot to an egress time slot **as a single traffic channel**.

13. **(Currently amended)** The method of Claim 12, further comprising:

writing a sub-channel in a fourth memory slot to a first disparate memory slot **associated with a third traffic channel**; and

writing a second sub-channel in the fourth memory slot to a second disparate memory slot **associated with a fourth traffic channel**.

14. **(Original)** The method of Claim 12, further comprising writing a sub-channel in a field of a fourth memory slot to a disparate field of one of the memory slots in the exchange memory.

15. **(Original)** The method of Claim 12, wherein the traffic channel is a DS-0 and the sub-channel is a ¼ DS-0.

16. **(Original)** The method of Claim 12, further comprising:

writing each traffic channel to a separate random access memory (RAM) slot in an exchange RAM;

writing a sub-channel in a first RAM slot to a first field in an exchange register of an exchange register bank; and

writing a sub-channel in a second RAM slot to a second field in the exchange register.

17. **(Original)** The method of Claim 16, wherein the exchange register is internal to a controller writing the sub-channels from the RAM slot to the exchange register.

18. **(Currently amended)** A switch card for a telecommunications node, comprising:

a time slot interchanger (TSI);

a switch interface operable to receive traffic from a plurality of line cards for the TSI and to transmit traffic from the TSI to the line cards;

an instruction register operable to provide predefined switching instructions to the TSI for routing traffic to and from the line cards;

an exchange register bank;

an exchange random access memory (RAM); and

the TSI responsive to the predefined switching instructions from the instruction register to write traffic channels received from the switch interface into the exchange RAM, to write a sub-channel **of a first channel that is stored** in a first slot of exchange RAM to a first field in an exchange register of the exchange register bank and to write a sub-channel **of a second channel that is stored** in a second slot of exchange RAM to a second field in the exchange register**, so that the sub-channel written to the first field and the sub-channel written to the second field may be read from the memory slot as a single traffic channel**.

19. **(Currently amended)** The switch card of Claim 18, the TSI further operable to write **a first sub-channel of a third channel that is stored in a third slot of the exchange RAM to a second exchange register associated with a fourth channel and to write a second sub-channel of the third channel to a third exchange register associated with a fifth channel**. ~~first and second sub-channels stored in a slot of the exchange RAM to disparate exchange registers.~~

20. **(Original)** The switch card of Claim 18, wherein the exchange register is internal to the TSI.

21. **(Currently amended)** A method for processing traffic in a time slot interchanger (TSI) comprising:

receiving a traffic stream **comprising** ~~**including**~~ a plurality of traffic channels;

writing each traffic channel to a memory slot in an exchange memory;

reading a traffic channel stored in a memory slot;

modifying data to generate a modified traffic channel; and

writing the modified traffic channel to a memory slot.

22. **(Original)** The method of Claim 21, further comprising modifying the data based on logic operations provided with an instruction word for the TSI.

23. **(Original)** The method of Claim 21, further comprising writing the modified traffic channel to a disparate traffic channel.

24. **(Original)** The method of Claim 21, further comprising:

determining a value of the data in the traffic channel; and

performing a specified action when the data has a specified value.

25. **(Original)** The method of Claim 21, further comprising merging data of the traffic channel with data from a disparate traffic channel to form a conference traffic channel.

26. **(Currently amended)** A system for time division multiplex (TDM) switching of traffic in a telephone node, comprising:

a computer-readable medium; and

software stored in the computer-readable medium, the software operable to receive a traffic stream **comprising** ~~including~~ a plurality of traffic channels **comprising** ~~including~~ discreet sub-channels, **to write a first traffic channel that includes a first sub-channel to a first memory slot in an exchange memory, to write a second traffic channel that includes a second sub-channel to a second memory slot in an exchange,** ~~to write each traffic channel to a separate memory slot in an exchange memory,~~ to write **the first sub-channel** ~~a sub-channel in a first memory slot~~ to the first field in the **third** ~~second~~ memory slot, to write **the second sub-channel** ~~a sub-channel in a second memory slot~~ to a second field in the **third** ~~second~~ memory slot, and to read ~~a combined traffic channel including~~ the sub-channels from the **third** ~~second~~ memory slot to an egress time slot.

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27. **(Currently amended)** The system of ~~Claim 25~~ **Claim 26**, the software further operable to write a sub-channel in a fourth memory slot to a first disparate memory slot **associated with a third traffic channel** and to write a second sub-channel in a fourth memory slot to a second disparate memory slot **associated with a fourth traffic channel**.

28. **(Currently amended)** The system of ~~Claim 25~~ **Claim 26**, the software further operable to write a sub-channel in a field of a fourth memory slot to a disparate field of one of the memory slots in the exchange memory.

29. **(Currently amended)** The system of ~~**Claim 25**~~ **Claim 26**, wherein the traffic channel is a DS-0 and the sub-channel is a ¼ DS-0.

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30. **(Currently amended)** The system of ~~**Claim 25**~~ **Claim 26**, the software further operable to write each traffic channel to a separate random access memory (RAM) slot in an exchange RAM, to write a sub-channel in a first RAM slot to a first field in an exchange register of an exchange register bank, and to write a sub-channel in a second RAM slot to a second field in the exchange register.

31. **(Currently amended)** A system for processing traffic in a time slot interchanger (TSI) comprising:

a computer-readable medium; and

software stored in the computer-readable medium, the software operable to receive a traffic stream **comprising** ~~**including**~~ a plurality of traffic channels, to write each traffic channel to a memory slot in an exchange memory, to read a traffic channel stored in a memory slot, to modify data to generate a modified traffic channel, and to write the modified traffic channel to a memory slot.

32. **(Previously presented)** The system of Claim 31, the software further operable to modify the data based on logic operations provided with an instruction word for the TSI.

33. **(Previously presented)** The system of Claim 31, the software further operable to write the modified traffic channel to a disparate traffic channel.

34. **(Previously presented)** The system of Claim 31, the software further operable to determine a value of the data in the traffic channel and to perform a specified action when the data has a specified value.

35. **(Previously presented)** The system of Claim 31, the software further operable to merge data of the traffic channel with data from a disparate traffic channel to form a conference traffic channel.

36. **(New)** A system for processing telecommunication traffic comprising:

means for receiving a traffic stream comprising a plurality of traffic channels having discrete sub-channels;

means for writing a first traffic channel that includes a first sub-channel to a first memory slot in an exchange memory;

means for writing a second traffic channel that includes a second sub-channel to a second memory slot in an exchange memory;

means for writing the first sub-channel to a first field in a third memory slot;

means for writing the second sub-channel to a second field in the third memory slot; and

means for reading the sub-channels from the third memory slot to an egress time slot as a single traffic channel.

37. **(New)** A system for processing telecommunication traffic comprising:

means for receiving a traffic stream comprising a plurality of traffic channels;

means for writing each traffic channel to a memory slot in an exchange memory;

means for reading a traffic channel stored in a memory slot;

means for modifying data to generate a modified traffic channel; and

means for writing the modified traffic channel to a memory slot.